

The Invention Claimed Is

1. A programmable logic device comprising:
  - a plurality of super-regions of programmable logic, each super-region comprising:
    - at least one region of programmable logic, each region comprising at least one subregion of programmable logic;
    - a memory region;
    - an inter-region interconnection conductor;
    - first interconnection circuitry configured to selectively interconnect at least one of the subregions with a region feeding conductor;
    - second interconnection circuitry configured to selectively interconnect the region feeding conductor and the inter-region interconnection conductor;
    - third interconnection circuitry configured to selectively interconnect the memory region and the inter-region interconnection conductor; and
    - the first, second, and third interconnection circuitry configured such that signals can be conveyed between the memory region and the at least one of the subregions; and
    - fast interconnection circuitry extending to all of the super-regions and configurable to receive a plurality of fast signals from a plurality of sources and to convey to each of a plurality of multiplicities of the super-regions selected ones of the fast signals.

2. The programmable logic device defined in claim 1 wherein the sources include a plurality of input pins.

3. The programmable logic device defined in claim 2 wherein the sources further include selected ones of the subregions.

4. The programmable logic device defined in claim 1 wherein the sources include selected ones of the subregions.

5. The programmable logic device defined in claim 4 wherein each of the multiplicities of the super-regions includes at least one of the selected ones of the subregions.

6. The programmable logic device defined in claim 1 wherein each subregion is programmable to perform a logic operation on an input signal applied to each subregion.

7. The programmable logic device defined in claim 1 wherein each subregion is programmable to perform a control operation on an input signal applied to each subregion.

8. The programmable logic device defined in claim 1 wherein the plurality of super-regions of programmable logic is arranged in a two-dimensional array of rows and columns.

9. The programmable logic device defined in claim 8, the fast interconnection circuitry comprising:

a plurality of horizontal super-region interconnection conductors associated with each of the rows of super-regions wherein each horizontal super-region interconnection conductor is programmable to couple any super-region in the associated row to another super-region in the associated row;

a plurality of vertical super-region interconnection conductors associated with each of the columns of super-regions wherein each vertical super-region interconnection conductor is programmable to couple any super-region in the associated column to another super-region in the associated column; and

a first plurality of programmable logic connectors configured to selectively interconnect the horizontal and vertical super-region interconnection conductors.

10. A digital processing system comprising:  
processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 1 coupled to the processing circuitry and the memory.

11. A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

12. The printed circuit board defined in claim 11 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic device.

13. The printed circuit board defined in claim 11 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic device.

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